Remarks

Claims 1-2 are pending in the application. Claims 1-2 are rejected. All rejections and objections are respectfully traversed.

Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over Buchanan et al., (U.S. 6,970,435 – Buchanan) in view of Partyka (U.S. 5,659,580).

The arguments asserted on June 3, 2008 in the Applicants response to the office action dated December 3, 2007 are incorporated herein by reference in their entirety and thereby re-asserted.

The invention generates lesser width parallel data words from a greater width parallel data word by interleaving bits of the greater width parallel data word across the lesser width parallel data words such that each successive bit of said greater width parallel data word is contained within a different one of said lesser width parallel data words. Buchanan describes partitioning a 16 bit data stream into four groups of four bit nibbles, see col. 4, lines 50-66, below:

> interface is on a byte (8-bit) boundary. According to the present invention, it is more advantageous to partition the bits into nibbles for processing and sending through the serial link. In one embodiment of the present invention, 16-bit parallel data streams are supplied to DASL interface. The bit streams are partitioned into four groups of four bit (4-bits=1 nibble) streams. Each of the nibbles is processed according to the teaching of the present invention and is sent over a serial link. As a consequence, to transmit the 16-bit, four serial links would be required. Each nibble of data is processed in the same way; therefore, the description of one (set forth hereinafter) is intended to cover the processing of the others. The four parallel data bit streams are transformed into a high speed serial bit stream by latching each of the four bit streams in one of the Latch L1 through L4 and sequentially strobing the latched information at four time the parallel clock rate using Multiplexer Circuit 22. The data

Therefore, Buchanan teaches partitioning a 16 bit parallel data word into 4 bit nibbles using one of latches L1-L4 for each nibble, and then sequentially strobing the latched nibbles using the multiplexer circuit 22.

In contrast, the invention generates lesser width parallel data words by interleaving bits of the greater width parallel data word across the lesser width parallel data words such that each successive bit of said greater width parallel data word is contained within a different one of said lesser width parallel data words. Then, the lesser width parallel data words are serialized and transmitted.

Partyka fails to cure the defects of Buchanan. Claimed is interleaving bits of the greater width parallel data word across the lesser width parallel data words such that each successive bit of said greater width parallel data word is contained within a different one of said lesser width parallel data words. In contrast, Partyka explicitly teaches interleaving ***contiguous buffer addresses*** to change an output transmission order of data bits in a single data block for transmission , see col. 4, lines 2-20, below:

ated by contiguous counter **214**. In other words, encoded data **142** is stored in contiguous order in data buffer **202**, i.e., bit **0** of encoded data stream **142** is stored in the first bit address location in data buffer **202**, bit **1** of the encoded data stream **142** is stored in the second bit address location, bit **2** of the encoded data stream **142** is stored in the third bit address location, etc.

After encoded data **142** is completely stored in data buffer **202**, multiplexer **210** connects address twister **216** to address bus **208** of data buffer **202**. Address twister **216** is a state machine which generates a noncontiguous sequence of addresses which corresponds to an interleaving sequence. Thus, encoded data **142** is output from data buffer **202** in an order defined by the interleaving sequence generated by address twister **216**. In other words, the interleaving sequence generated by address twister **216** is used to address data buffer **202** as encoded data **142** is output from data buffer **202**. Thus, data is output from data buffer **202** in a sequence that corresponds to the interleaving sequence generated by address twister **216**.

Partyka teaches a method for re-ordering data in a serial transmission. The Examiner has repeatedly referenced serial transmission schemes to attempt to teach the claimed ***parallel word generation*** according to the invention. A person of ordinary skill in the art would readily understand that the invention generates lesser width parallel words by interleaving bits of a greater width parallel data word according to the claims. Partyka has nothing to with parallel data words, as claimed. Partyka reorders bits of a data block for transmission by interleaving contiguous buffer addresses. Therefore, the rejection should be reconsidered and withdrawn.

Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Buchanan in view of Nishida, et al., (U.S. 5,978,486 – "Nishida").

The arguments asserted on June 3, 2008 in the Applicants response to the office action dated December 3, 2007 are incorporated herein by reference in their entirety and thereby re-asserted.

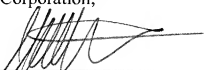
As stated in the previous response, the best the Examiner could hope to teach with the combination of Buchanan and Nikida is scrambling partitioned parallel data. As stated above with respect to claim 1, Partyka teaches re-ordering serial data to output from a buffer by interleaving contiguous buffer addresses. Therefore, a person of ordinary skill in the art would readily understand that Partyka's serial re-ordering has nothing to do with generating lesser width parallel data words from a greater width parallel data word, as claimed.

Further, there is no motivation to combine Buchanan with either Nishida or Partyka in any of the references. The Examiner's alleged motivation to combine the references, and his supportive reference to Buchanan at col. 1, lines 26-29, is non-sequitor.

It is believed that this application is now in condition for allowance. A notice to this effect is respectfully requested. Should further questions arise concerning this application, the Examiner is invited to call Applicant's attorney at the number listed below.

Please charge any shortage in fees due in connection with the filing of this paper to Deposit Account 50-3650.

Respectfully submitted,
3Com Corporation,

By 

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